PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Vernon M. Williams

Serial No.: 09/511,986

Filed: February 24, 2000

For: STEREOLITHOGRAPHICALLY FABRICATED CONDUCTIVE ELEMENTS, SEMICONDUCTOR DEVICE COMPONENTS AND ASSEMBLIES INCLUDING SUCH CONDUCTIVE ELEMENTS, AND METHODS

Confirmation No.: 6129

Examiner: O. Nadav

Group Art Unit: 2811

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VIA ELECTRONIC FILING
April 7, 2008

APPEAL BRIEF

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: Board of Patent Appeals and Interferences

Sir:

This Appeal Brief is being submitted in the format required by 37 C.F.R. § 41.37(c)(1), the fee required by 37 C.F.R. § 41.20(b)(2) having been paid on September 24, 2004, when the original Appeal Brief was filed in the above-referenced application.

This Supplemental Appeal Brief is being filed in response to the new grounds of rejection presented in the Office Action dated November 9, 2004, the three-month shortened statutory period for response to which is set to expire on February 9, 2005.

By filing this Supplemental Appeal Brief, Applicants respectfully request reinstatement of the appeal of the Examiner's final rejections of the claims of the above-referenced application.

I. REAL PARTY IN INTEREST

U.S. Application Serial No. 09/511,986 (hereinafter "the '986 Application"), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc., as evidenced by the assignment that has been recorded with the U.S. Patent & Trademark Office (hereinafter "the Office") at Reel No. 010636, Frame No. 0779. Accordingly, Micron Technology, Inc., is the real party in interest in the above-referenced appeal.

II. RELATED APPEALS AND INTERFERENCES

Neither Appellant nor the undersigned attorney is currently aware of any appeals or interference proceedings that would affect or be affected by the Board's decision in the above-referenced appeal.

III. STATUS OF CLAIMS

Claims 47, 48, 50-56, 58-68, 75-90, and 110-124 are currently pending in the above-referenced application.

Claims 47, 48, 50-56, 58-68, 75-79, 81-85, and 110-124 have been considered.

Claims 80 and 86-90 have been withdrawn from consideration for being drawn to a nonelected species of invention.

No claims have been allowed.

The rejections of claims 47, 48, 50-56, 58-68, 75-79, 81-85, and 110-124 are being appealed.

IV. STATUS OF AMENDMENTS

The '986 Application was filed on February 24, 2000, with one-hundred-nine (109) claims.

On March 9, 2001, the Office made a Restriction Requirement in the '986 Application.

A Response to the Restriction Requirement, in which an election was made, without traverse, to prosecute claims 47-105, was filed on March 27, 2001.

An Election of Species Requirement followed on April 20, 2001.

On May 11, 2001, a Response to Election of Species Requirement and Preliminary Amendment was filed.

On June 19, 2001, the Office sent a communication indicating that the Response to Election of Species Requirement and Preliminary Amendment was not fully responsive, asserting that the Response was not in compliance with various formalities.

A revised Response and Preliminary Amendment, which addressed the prior informalities, was filed on July 5, 2001.

The first Office Action on the merits of the claims, which indicated that claims 69-74 and 91-109 had also been withdrawn from consideration, was mailed on August 9, 2001. Each of claims 47-68 and 75-90 was rejected in the Office Action of August 9, 2001.

An Amendment was filed on November 13, 2001, with a petition and the fee for a one-month extension of time, to respond to the rejections presented in the Office Action of August 9, 2001. In the Amendment of November 13, 2001, all of the claims that had been withdrawn from consideration (*i.e.*, claims 1-46, 69-74, and 91-109) were canceled without prejudice or disclaimer. Various claim amendments were also presented, as were explanations as to the patentability of claims 47-68 and 75-90.

A Final Office Action followed on January 7, 2002. All of the previously-presented claim rejections were maintained in the Final Office Action.

On March 7, 2002, an Amendment Under 37 C.F.R. § 1.116 was filed. Further claim amendments (including the cancellation of claims 49 and 57) and remarks were presented in that Amendment.

As indicated in the Advisory Action dated March 19, 2002, the Examiner refused to enter the claim revisions that had been proposed in the Amendment Under 37 C.F.R. § 1.116.

On March 26, 2002, a Request for Continued Examination ("RCE") was filed, requesting entry of the claim revisions that were presented in the Amendment Under 37 C.F.R. § 1.116.

During a telephone conference on May 1, 2002, claims 80 and 86-90 were withdrawn from consideration as being directed to a nonelected species of invention.

On May 6, 2002, a third Office Action on the merits of the claims was mailed. Each of claims 47, 48, 50-56, 58-68, 75-79, and 81-85, which remained under consideration, was rejected. Notably, the prior grounds of rejection had been withdrawn.

A response to the Office Action of May 6, 2002, in the form of an Amendment, was filed on August 6, 2002. New claims 110-124 (which were improperly numbered as claims 91-105 at the time) were added. Some claim revisions were also presented, as was reasoning in support of the patentability of the pending claims.

On February 11, 2003, the Office mailed a Notice of Abandonment for failure to respond to the Office Action of May 6, 2002. The Notice of Abandonment was totally unexpected, as an appropriate response had been filed.

On February 20, 2003, a Petition to Withdraw Holding of Abandonment was filed.

The Petition was promptly granted and the Notice of Abandonment vacated, as evidenced by a decision of the Special Programs Examiner for Technology Center 2800, which was dated May 1, 2003.

In a Final Office Action dated June 25, 2003, the rejections of claims 47, 48, 50-56, 58-68, 75-79, and 81-85 were maintained. Claims 110-124 were also rejected.

On August 25, 2003, another RCE and an Amendment were filed. Further claim amendments were presented in the Amendment of August 25, 2003.

Another Office Action on the merits was mailed on November 3, 2003. The rejections of claims 47, 48, 50-56, 58-68, 75-79, 81-85, and 110-124 were again maintained.

On February 6, 2003, another Amendment was filed. While many of the claims were revised, the revisions were merely formal. The Amendment of February 6, 2004, included

additional remarks and explanations as to the patentability of each of claims 47, 48, 50-56, 58-68, 75-79, 81-85, and 110-124. These were the last claim amendments that were introduced in the above-referenced application.

In a Final Office Action dated April 22, 2004, some of the prior claim rejections were finally withdrawn, while others were maintained.

A Response to Final Office Action was filed on June 28, 2004. Further explanations as to the patentability of the claims were provided.

Nonetheless, the Examiner maintained the rejections of claims 47, 48, 50-56, 58-68, 75-79, 81-85, and 110-124, as evidenced by the Advisory Action and accompanying remarks of July 12, 2004.

Accordingly, a Notice of Appeal was filed on July 15, 2004. The Notice of Appeal was followed by an Appeal Brief, which was filed on October 15, 2004, with a petition and the fee for a one-month extension of time.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The above-referenced application includes claims that are directed to conductive traces of semiconductor device components. The conductive trace 20 of independent claim 47 includes a plurality of superimposed, contiguous, mutually adhered layers 20A, 20B, each of which comprises conductive material, such as a conductive polymer. Fig. 13; page 8, lines 5-11. At least a portion of each conductive trace 20 is configured to extend and conduct electrical signals along a plane which is parallel to a plane in which the at least one semiconductor device component is located. *See* Fig. 13; page 8, lines 17-22.

Independent claim 52 of the above-referenced application is drawn to a semiconductor device component 10/30 that includes a conductive trace 20 with a plurality of superimposed, contiguous, mutually adhered layers 20A, 20B, each of which comprises conductive material, such as a conductive polymer. Fig. 13; page 8, lines 5-11. At least a portion of each conductive trace 20 is configured to extend and conduct electrical signals along a plane which is parallel to a plane in which the at least one semiconductor device component is located. *See* Fig. 13; page 8, lines 17-22.

The semiconductor device assembly 1 of independent claim 64 includes a carrier 30 and at least one semiconductor die 10. Figs. 1 and 2; page 28, line 25, to page 29, line 13. Contacts 32 of the carrier 30 and corresponding bond pads 12 of the semiconductor die 10 are electrically connected to one another by way of conductive traces 20. *Id.* Each conductive trace 20 includes a plurality of superimposed, contiguous, mutually adhered layers 20A, 20B, each of which comprises conductive material. Fig. 13; page 8, lines 5-11.

Independent claim 75 also recites a semiconductor device assembly. The semiconductor device assembly of independent claim 75 includes a first semiconductor device component 10 with a first contact pad 12, as well as a second semiconductor device component 10′ with a second contact pad 12′. *See, e.g.*, Figs. 3 and 4; page 29, line 14, to page 30, line 7. At least one conductive element 20 contacts both the first contact pad 10 and the second contact pad 10′. *See, e.g., id.* The at least one conductive element 20 includes a plurality of superimposed, contiguous, mutually adhered layers 20A, 20B, each of which comprises conductive material. Fig. 13; page 8, lines 5-11.

The conductive trace 20 of independent claim 110 includes a plurality of superimposed, contiguous, mutually adhered layers 20A, 20B, each of which comprises the same conductive material, such as a conductive polymer. Fig. 13; page 8, lines 5-11. At least a portion of each conductive trace 20 is configured to extend and conduct electrical signals along a plane which is parallel to a plane in which the at least one semiconductor device component is located. *See* Fig. 13; page 8, lines 17-22.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) Claims 64-66, 68, 75, 77-79, and 81-83 stand rejected under 35 U.S.C. § 102(e) for reciting subject matter which is allegedly anticipated by the subject matter described in U.S. Patent 5,969,424 to Matsuki et al. (hereinafter "Matsuki");

(B) Claims 47, 50-54, 58, 59, 62, 63, 110, 112-116, 119, 120, 123, and 124 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over teachings from U.S. Patent 4,610,941 to Sullivan (hereinafter "Sullivan") in view of teachings from U.S. Patent 4,752,498 to Fudim. The Office Action of November 9, 2004, indicates that these references may, in the alternative, be relied upon in a rejection of the claims under 35 U.S.C. § 102(b), but such a rejection is not permissible, as the Office relies on the teachings of both of the references in support of its assertions that all of the claim limitations are taught or suggested. M.P.E.P. § 2131.01.

(C) Claims 48, 55, 56, 60, 61, 111, 117, 118, 121, and 122 have been rejected under 35 U.S.C. § 103(a) for being drawn to subject matter which is assertedly unpatentable over

teachings from Sullivan, in view of the subject matter taught in Fudim and, further, in view of teachings from U.S. Patent 4,954,873 to Lee et al. (hereinafter "Lee");

(D) Claims 67 and 76 have both been rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly nonobvious over the subject matter taught in Matsuki, in view of teachings from Lee; and

(E) Claims 75, 84, and 85 are rejected under 35 U.S.C. § 103(a) for being directed to subject matter which is assertedly unpatentable over the teachings of U.S. Patent 5,007,576 to Congleton et al. (hereinafter "Congleton"), in view of teachings from Matsuki.

VII. ARGUMENT

A. REJECTIONS UNDER 35 U.S.C. § 102(e)

Claims 64-66, 68, 75, 77-79, and 81-83 stand rejected under 35 U.S.C. § 102(e) for reciting subject matter which is purportedly anticipated by the subject matter described in Matsuki.

1. APPLICABLE LAW

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

2. REFERENCE RELIED UPON

The description of Matsuki is directed to semiconductor devices with redistribution layers (RDLs) formed thereon. More specifically, as shown in FIG. 2 of Matsuki, a semiconductor device according to Matsuki includes bond pads 4 on an active surface thereof. An RDL formed on the active surface of the semiconductor device includes a first protective insulation substrate 5, through which the bond pads 4 are exposed. Lead wires 7 of the RDL, which include first, second, and third conductive layers 13, 15, and 16, respectively, contact each bond pad 4 and extend laterally therefrom, over the first protective insulation substrate 5. Col. 7, line 65, to col. 8, line 61; *more specifically,* col. 8, lines 60 and 61. A second protective insulation substrate 8 of the RDL covers all but a terminal end of each lead wire 7 (col. 8, lines 62-65), which is opposite from the end of the lead wire 7 that contacts the corresponding bond pad 4 (*see* FIG. 2). The terminal end of each lead wire 17 is referred to in Matsuki as a "secondary pad 17." Col. 8, lines 65-67. The exposed, secondary pad 17 portion of each lead wire 7 serves as a redistributed bond pad. *See* FIG. 2.

A solder ball 10 that has been secured to the exposed, secondary pad 17 portion of a lead wire 7 of the RDL of Matsuki electrically connects the bond pad 4 of the semiconductor device described therein to a corresponding contact 11 of a carrier 12, as shown in FIG. 2 of Matsuki, but does not contact the corresponding contact 11 of the carrier 12. Col. 9, lines 2-18. Alternatively, as described at col. 9, lines 15 and 16, a bond wire may be secured directly to the secondary pad 17 portion of the lead wire 7 and to establish electrical communication between the lead wire 7 and a corresponding contact 11 of a carrier 12.

It is apparent that Matsuki lacks any express or inherent description, or any teaching or suggestion, that the multi-layered lead wires 7 described therein may be used in any capacity other than as conductive traces within a redistribution layer of a single semiconductor device.

3. ANALYSIS

(a) Claims 64-66 and 68

Independent claim 64 is drawn to a semiconductor device assembly which includes a carrier, at least one semiconductor die adjacent to the carrier, and conductive elements. Each conductive element includes a plurality of superimposed, contiguous, mutually adhered layers of conductive material. The conductive elements extend between and contact contacts of the carrier and their corresponding bond pads of the at least one semiconductor device.

While the lead wires 7 of Matsuki contact a bond pad 4 of a semiconductor device, they do *not contact* a contact 11 of the carrier 12. Rather, as col. 9, lines 2-18 of Matsuki quite clearly explains, an intervening solder ball 10 or bond wire (not shown) is required to establish communication between each lead wire 7 and its corresponding contact 11 of a carrier 12. Therefore, Matsuki does not expressly or inherently describe a semiconductor device assembly that includes conductive elements that extend between and *contact* contacts of a carrier and bond pads of a semiconductor die, as required by independent claim 64.

Moreover, Matsuki does not include any express or inherent description that the solder ball 11 or bond wire that has been positioned between the secondary pad 17 portion of each lead wire 7 of a semiconductor device and its corresponding contact 11 of a carrier includes a plurality of superimposed, contiguous, mutually adhered layers. Therefore, Matsuki does not anticipate a

conductive element that includes a plurality of superimposed, contiguous, mutually adhered layers *and* contacts both bond pad 4 and contact 11.

As Matsuki does not anticipate each and every element of independent claim 64, it is respectfully submitted that, under 35 U.S.C. § 102(e), independent claim 64 is allowable over the subject matter described in Matsuki.

Each of claims 65, 66, and 68 is allowable, among other reasons, for depending from claim 64, which is allowable.

(b) Claims 75-77, 79, and 81-83

Independent claim 75 recites a semiconductor device assembly. The semiconductor device assembly of independent claim 75 includes first and second semiconductor device components and at least one conductive element. Each of the first and second semiconductor device components includes at least one contact pad. The at least one conductive element contacts both the at least one first contact pad of the first semiconductor device component and the at least one second contact pad of the at least one second semiconductor device component.

Again, Matsuki lacks any express or inherent description that the lead wire 7 thereof contacts both the bond pad 4 of the semiconductor device thereof and the contact 11 of the carrier 12 thereof. Instead, as shown in FIG. 2 and explained at col. 9, lines 2-18 of Matsuki, a solder ball 10 or bond wire (not shown) is positioned between the lead wire 7 and the contact 11 to facilitate electrical communication therebetween.

Because Matsuki does not anticipate each and every element of independent claim 75, it is respectfully submitted that, under 35 U.S.C. § 102(e), independent claim 75 is allowable over Matsuki.

Claims 77-79 and 81-83 are each allowable, among other reasons, for depending either directly or indirectly from claim 75, which is allowable.

Claim 82 is further allowable since Matsuki does not include any express or inherent description that carrier 12 thereof includes a conductive trace that is carried by a support structure thereof and that is in communication with contact 11.

Claim 83, which depends from claim 82, is additionally allowable since Matsuki lacks any express or inherent description that either a support structure or a conductive trace of the carrier 12 thereof includes a plurality of superimposed, contiguous, mutually adhered layers. Rather, the Matsuki merely describes a lead wire 7 that includes multiple layers 13, 15, 16.

For these reasons, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 64-66, 68, 75, 77-79, and 81-83 be reversed.

B. REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 47, 48, 50-56, 58-63, 67, 75, 76, 84, 85, and 110-124 stand rejected under 35 U.S.C. § 103(a).

1. APPLICABLE LAW

M.P.E.P. 706.02(j) sets forth the standard for a rejection under 35 U.S.C. § 103(a):

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant=s disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

2. ADDITIONAL REFERENCES RELIED UPON

Sullivan

Sullivan teaches, among other things, a printed wiring board that includes metallic conductors 15 on a surface thereof, as well as a temporary photopolymer layer 11 over the surface, including the metallic conductors 15. FIGs. 1 and 2; col. 4, lines 19-29. Sullivan does not teach or suggest that the metallic conductors 15 include more than one material layer or that they may be formed from a conductive polymer.

Fudim

Fudim teaches a technique that may be used to fabricate circuit boards. Col. 5, lines 58-60. The method of Fudim includes sequentially forming multiple layers from a UV-curable material, then using conventional metallization techniques to form conductive layers of the circuit board. Col. 5, lines 60-64. Fudim also discloses that conductive layers and structures, as well as electrical components, may be embedded within a circuit board during

fabrication thereof. Col. 6, lines 10-25. Fudim does not teach or suggest that the techniques disclosed therein may be used to fabricate conductive structures, however.

Lee

Lee teaches an anisotropic (*i.e.*, z-axis) elastomeric conductor that is formed by slicing a block formed from a plurality of stacked sheets. *See, e.g.*, FIG. 1. The block includes sheets with parallel electrically conductive fibers that have been interspersed between sheets formed from an insulative material. *See, e.g.*, FIGs. 1 and 4; col. 4, line 55, to col. 5, line 34. An elastomer is introduced into the stacked sheets. Col. 5, lines 35-59. Once the elastomer hardens or cures, the block is sliced along planes that are oriented transversely (*e.g.*, perpendicularly) to the planes in which the sheets of the block are located. FIG. 4; col. 5, line 60, to col. 6, line 6. Each anisotropic conductor that has been formed in this manner thus includes conductive elements 14 which extend perpendicular to a plane of the anisotropic conductor. FIGs. 4-6; col. 5, line 60, to col. 6, line 2.

Congleton

Congleton teaches, among other things, the use of ribbon or wire leads 16 to connect contacts 10a of a semiconductor device 10 to corresponding contacts 12b, 12c, 12d of a circuit board 12. Congleton does not teach or suggest that these leads may include more than one layer of conductive material.

3. ANALYSIS

(a) Sullivan in View of Fudim

Claims 47, 50-54, 58, 59, 62, 63, 110, 112-116, 119, 120, 123, and 124 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over teachings from Sullivan, in view of teachings from Fudim.

Independent claim 47 is directed to a conductive trace that includes a plurality of superimposed, contiguous, mutually adhered layers, each of which comprises the same conductive polymer.

Independent claim 52 recites a semiconductor device that includes a semiconductor device component and at least one conductive trace. The at least one conductive trace includes a plurality of superimposed, contiguous, mutually adhered layers. Each of the layers comprises a conductive polymer.

Independent claim 110 is also drawn to a conductive trace that includes a plurality of superimposed, contiguous, mutually adhered layers. Each of the layers comprises conductive polymer, but different layers need not comprise the same conductive polymer.

Independent claim 114 recites a semiconductor device that includes a semiconductor device component and at least one conductive trace. The at least one conductive trace includes a plurality of superimposed, contiguous, mutually adhered layers. Each of the layers comprises the same conductive polymer.

The Examiner has apparently disregarded the "plurality of . . . layers" language in independent claims 47, 52, 110, and 114 by stating that such layers would be "indistinguishable from one another, and thus can be considered as one layer." The Examiner has ignored the law,

which requires that each and every element of a claim be taught or suggested by the art in order for a claim to be rendered unpatentable under 35 U.S.C. § 103(a). Independent claims 47, 52, 110, and 114 require a plurality of superimposed, contiguous, mutually adhered layers. Neither Sullivan nor Fudim teaches or suggests a conductive trace that includes a plurality of superimposed, contiguous, mutually adhered layers. Therefore, Sullivan and Fudim, taken individually or collectively, do not teach or suggest each and every element of independent claims 47, 52, 110, and 114.

Even assuming, *arguendo,* that the Examiner were entitled to overlook the law, neither Sullivan nor Fudim, taken either together or separately, teaches or suggests a conductive trace that comprises a conductive polymer, as is required by independent claims 47, 52, 110, and 114.

For these reasons, the Examiner has not established a *prima facie* case of obviousness against independent claim 47, independent claim 52, independent claim 110, or independent claim 114, as would be required to maintain the 35 U.S.C. § 103(a) rejection of these claims.

Claims 50 and 51 are both allowable, among other reasons, for depending directly from claim 47, which is allowable.

Each of claims 53, 54, 58, 59, 62, and 63 is allowable, among other reasons, for depending directly or indirectly from claim 52, which is allowable.

Claims 112 and 113 are both allowable, among other reason, for depending directly from claim 110, which is allowable.

Claims 115, 116, 119, 120, 123, and 124 are each allowable, among other reason, for depending either directly or indirectly from claim 114, which is allowable.

In view of the foregoing, reversal of the 35 U.S.C. § 103(a) rejection of claims 47, 50-54, 58, 59, 62, 63, 110, 112-116, 119, 120, 123, and 124 is respectfully requested

(b) Sullivan, Fudim, and Lee

Claims 48, 55, 56, 60, 61, 111, 117, 118, 121, and 122 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over that taught in Sullivan, in view of teachings from Fudim and, further, in view of the teachings of Lee.

Claim 48 is allowable, among other reasons, for depending from claim 47, which is allowable.

Claims 55, 56, 60, and 61 are each allowable, among other reasons, for depending directly or indirectly from claim 52, which is allowable.

Claim 111 is allowable, among other reasons, for depending directly from claim 110, which is allowable.

Each of claims 117, 118, 121, and 122 is allowable, among other reasons, for depending directly or indirectly from claim 110, which is allowable.

Accordingly, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 48, 55, 56, 60, 61, 111, 117, 118, 121, and 122 be reversed.

(c) Matsuki in View of Lee

Claims 67 and 76 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over that taught in Matsuki, in view of teachings from Lee.

It is respectfully submitted that a *prima facie* case of obviousness has not been established against either claim 67 or claim 76 for at least two reasons.

First, it is respectfully submitted that the anisotropic elastomeric conductors of Lee could not be used to form the lead wires of Matsuki and, thus, that one of ordinary skill in the art would have no reason to expect the asserted combination of teachings from Matsuki and Lee to be successful. In particular, the anisotropic elastomeric conductors of Lee are sheets with conductive elements that extend transversely (*e.g.*, perpendicularly) relative to the planes thereof, not laterally along the planes. If the anisotropic elastomeric conductors of Matsuki were to be used as the lead wires 7 of the assembly taught in Matsuki, the conductive elements would only be able to conduct electricity between the upper and lower surfaces of the lead wires 7, not along the lengths thereof. Thus, electricity could not be communicated from a bond pad 4 at one end of such a lead wire 7 to a secondary pad 17 at the other, terminal end of the lead wire 7. Nonetheless, Matsuki requires that electricity be conducted along the lengths of lead wires 7 to establish communication between bond pads 4 and contacts 11.

For this reason, one of ordinary skill in the art would have had no reason to expect that the asserted combination of teachings from Matsuki and Lee would have been successful.

Second, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Matsuki and Lee in the manner that has been asserted. In particular, the teachings of Matsuki are limited to redistribution layers that include *metal* lead wires 7 that extend and conduct electric signals along planes that are substantially parallel to a plane in which the underlying semiconductor devices are located. Lee, in contrast, teaches anisotropic elastomeric conductors. When an anisotropic elastomeric conductor of Lee is

used with a semiconductor device, as shown in FIG. 5 of Lee, the conductive elements thereof are oriented perpendicularly relative to a plane in which the semiconductor device is located. Thus, the conductive elements of the anisotropic elastomeric conductor of Lee conduct electrical signals in a direction which is perpendicular to the plane in which an adjacent semiconductor device is located (*i.e.,* only between the top and bottom surfaces of the planar anisotropic elastomeric conductor). In view of these divergent teachings, it is not understood how, other than on the improper basis of hindsight provided by the teachings of the above-referenced application, one of ordinary skill in the art would have been motivated to combine the teachings of Matsuki and Lee in such a way as to render obvious the recitation of conductive elements that comprise conductive polymer and that are at least partially "configured to extend and conduct electrical signals along a plane which is parallel to a plane in which . . . at least one semiconductor device component is located" in independent claims 47, 52, 110, and 114.

Therefore, it is respectfully submitted that a *prima facie* case of obviousness has not been established against either claim 67 or claim 76 and that, under 35 U.S.C. § 103(a), both of these claims are directed to subject matter which is allowable over the teachings of Matsuki and Lee.

Accordingly, reversal of the 35 U.S.C. § 103(a) rejections of claims 67 and 76 is respectfully requested.

(d) Congleton in View of Matsuki

Claims 75, 84, and 85 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over that taught in Congleton, in view of teachings from Matsuki.

It is respectfully submitted that the teachings of Congleton and Matsuki do not support a *prima facie* case of obviousness against independent claim 75 because one of ordinary skill in the art would not have been motivated to combine the teachings of these references in the manner that has been asserted. Specifically, Congleton teaches semiconductor device assemblies which include leads positioned between the contacts of a semiconductor die and a carrier. The contacts of both the semiconductor die and the carrier of Congleton are exposed. More specifically, as shown in Fig.1.b. of Congleton, the contacts 10a of a semiconductor device component, referred to as "component 10," are shown as being exposed at the upper surface thereof, while corresponding contacts 12c of a test substrate 12 are exposed laterally beyond the outer periphery of component 10. This configuration permits leads 16 to be secured between corresponding pairs of contacts 10a and 12c. In contrast, Matsuki teaches that the bond pads 4 of the semiconductor die thereof and the contacts 11 of the carrier 12 taught therein are to be sandwiched between the semiconductor die and the carrier, not exposed to the exterior of such an assembly. Thus, it would be difficult, if not impossible, to directly connect leads such as those described in Congleton to both the bond pads 4 and the contacts 11.

Moreover, Congleton does not teach or suggest that these leads may include more than one layer of conductive material. While Matsuki teaches lead wires 7 that include multiple layers 13, 15, 16 of conductive material, the teachings of Matsuki are limited to use of the lead wires 7 *within* in a redistribution layer of a semiconductor device. The lead wires 7 are, in fact, fabricated as part of the redistribution layer and do not extend beyond the outer periphery of the resulting semiconductor device package.

For these reasons, it is respectfully submitted that none of Matsuki, Congleton, or the knowledge that was generally available in the art before the filing date of the above-referenced application would have provided one of ordinary skill in the art with the requisite motivation to use multi-layered lead wires 7, such as those taught in Matsuki, in the assembly of Congleton.

Moreover, as the use of photoresists, as employed in the method taught in Matsuki, is typically very expensive, one of ordinary skill in the art would not have been motivated to use the processes that are taught in Matsuki to form an assembly in accordance with the teachings of Congleton.

Due to these differences between Congleton and Matsuki, it is further submitted that any motivation to combine the teachings of Congleton and Matsuki in the manner that has been asserted could only have been improperly gleaned from the hindsight provided by the disclosure of the above-referenced application.

It is, therefore, respectfully submitted that, under 35 U.S.C. § 103(a), independent claim 75 is allowable over the teachings of Congleton and Matsuki.

Claims 84 and 85 are both allowable, among other reasons, as depending either directly or indirectly from claim 75, which is allowable.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 75, 84, and 85 be reversed.

3. ELECTION OF SPECIES REQUIREMENT

It is respectfully submitted that claim 75 remains generic to both species of invention that have been identified by the Office. Accordingly, consideration and allowance of claims 80 and 86-90 is respectfully requested. M.P.E.P. § 806.04(d).

VIII. CLAIMS APPENDIX

The current status of each claim that has been introduced into the above-referenced application is set forth in CLAIMS APPENDIX to this Appeal Brief.

IX. EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132. Accordingly, no evidence appendix accompanies this Appeal Brief.

X. RELATED PROCEEDINGS APPENDIX

No decisions have been rendered by the Board or any court in a related proceeding/application. Therefore, this Appeal Brief is not accompanied by a related proceedings appendix.

XI. CONCLUSION

It is respectfully submitted that:

(A) Claims 64-66, 68, 75, 77-79, and 81-83 are each allowable under 35 U.S.C. § 102(e) for reciting subject matter which is not anticipated by the disclosure of Matsuki;

(B) Claims 47, 50-54, 58, 59, 62, 63, 110, 112-116, 119, 120, 123, and 124 are each allowable under 35 U.S.C. § 103(a) for reciting subject matter which is patentable over teachings from Sullivan, in view of teachings from Fudim;

(C) Claims 48, 55, 56, 60, 61, 111, 117, 118, 121, and 122 recite subject matter which, under 35 U.S.C. § 103(a), is patentable over the subject matter taught in Sullivan, Fudim, and Lee, taken separately or in combination;

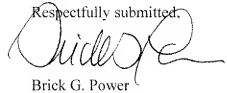
(D) Claims 67 and 76 are both allowable under 35 U.S.C. § 103(a) for reciting subject matter which is nonobvious over the subject matter taught in Matsuki and Lee;

(E) Claims 75, 84, and 85 are allowable under 35 U.S.C. § 103(a) for being directed to subject matter which is patentable over the teachings of Congleton and Matsuki; and

(D) Claims 80 and 86-90, which were withdrawn from consideration pursuant to a species election requirement, should be considered and allowed, as independent claim 75 is generic to both the elected species and the species to which claims 80 and 86-90 belong.

Accordingly, the rejections of claims 47, 48, 50-56, 58-68, 75-79, 81-85, and 110-124 should be reversed, and each of these claims, as well as claims 80 and 86-90, should be allowed.

Respectfully submitted,



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CLAIMS APPENDIX

1-46. (canceled)

47. (Previously presented) A conductive trace at least partially formed on at least one semiconductor device component, comprising a plurality of superimposed, contiguous, mutually adhered layers, each of the layers comprising conductive polymer, at least a portion of the conductive trace being configured to extend and conduct electrical signals along a plane which is parallel to a plane in which the at least one semiconductor device component is located.

48. (Previously presented) The conductive trace of claim 47, wherein the conductive polymer comprises a thermoplastic conductive elastomer.

49. (canceled)

50. (Previously presented) The conductive trace of claim 47, configured to be carried by a single semiconductor device component.

51. (Previously presented) The conductive trace of claim 47, configured to at least partially electrically connect two semiconductor device components.

52. (Previously presented) A semiconductor device comprising:

a semiconductor device component; and

at least one conductive trace carried by the semiconductor device component, the at least one conductive trace including a plurality of superimposed, contiguous, mutually adhered layers, each of the layers comprising conductive polymer, at least a portion of the at least one conductive trace being configured to extend and conduct electrical signals along a plane which is parallel to a plane in which the at least one semiconductor device component is located.

53. (Previously presented) The semiconductor device of claim 52, wherein the at least one conductive trace is substantially entirely carried by the semiconductor device component.

54. (Previously presented) The semiconductor device of claim 53, wherein the semiconductor device component comprises a layer of a carrier substrate.

55. (Previously presented) The semiconductor device of claim 53, wherein the semiconductor device component comprises a dielectric layer disposed on an active surface of a semiconductor die.

56. (Previously presented) The semiconductor device of claim 52, wherein the conductive polymer comprises a thermoplastic conductive elastomer.

57. (canceled)

58. (Previously presented) The semiconductor device of claim 52, wherein the at least one conductive trace communicates with a contact of the semiconductor device component.

59. (Previously presented) The semiconductor device of claim 58, wherein the semiconductor device component comprises a carrier substrate.

60. (Previously presented) The semiconductor device of claim 58, wherein the semiconductor device component comprises a semiconductor die.

61. (Previously presented) The semiconductor device of claim 58, wherein the semiconductor device component comprises a packaged semiconductor device.

62. (Previously presented) The semiconductor device of claim 52, wherein the semiconductor device component comprises leads.

63. (Previously presented) The semiconductor device of claim 62, wherein the at least one conductive trace contacts one of the leads.

64. (Previously presented) A semiconductor device assembly, comprising:
a carrier including contacts and carrying circuitry in communication with the contacts; and
at least one semiconductor die adjacent the carrier, the semiconductor die including bond pads; and

conductive elements extending between and contacting contacts of the carrier and corresponding bond pads to electrically connect circuitry of the at least one semiconductor die with the circuitry of the carrier, each of the conductive elements including a plurality of superimposed, contiguous, mutually adhered layers, each of the layers comprising conductive material.

65. (Previously presented) The semiconductor device assembly of claim 64, wherein the carrier comprises a carrier substrate.

66. (Previously presented) The semiconductor device assembly of claim 64, wherein the carrier comprises leads.

67. (Previously presented) The semiconductor device assembly of claim 64, wherein the conductive material comprises a thermoplastic conductive elastomer.

68. (Previously presented) The semiconductor device assembly of claim 64, wherein the conductive material comprises a metal.

69-74. (canceled)

75. (Previously presented) A semiconductor device assembly, comprising:

a first semiconductor device component including at least one first contact pad;

a second semiconductor device component including at least one second contact pad; and

at least one conductive element in contact with both the at least one first contact pad and the at least one second contact pad, the at least one conductive element comprising a plurality of superimposed, contiguous, mutually adhered layers comprising conductive material.

76. (Previously presented) The semiconductor device assembly of claim 75, wherein the conductive material comprises a conductive elastomer.

77. (Previously presented) The semiconductor device assembly of claim 75, wherein the conductive material comprises a metal.

78. (Previously presented) The semiconductor device assembly of claim 75, wherein at least one of the first semiconductor device component and the second semiconductor device component comprises a semiconductor die.

79. (Previously presented) The semiconductor device assembly of claim 78, wherein at least one of the first semiconductor device component and the second semiconductor device component comprises a packaged semiconductor die.

80. (Withdrawn) The semiconductor device assembly of claim 75, wherein each of the first semiconductor device component and the second semiconductor device component comprises at least one semiconductor die.

81. (Previously presented) The semiconductor device assembly of claim 75, wherein at least one of the first semiconductor device component and the second semiconductor device component comprises a carrier substrate.

82. (Previously presented) The semiconductor device assembly of claim 81, wherein the carrier substrate includes a support structure and at least one conductive trace carried by the support structure and in communication with the at least one first contact pad thereof.

83. (Previously presented) The semiconductor device assembly of claim 82, wherein at least one of the at least one conductive trace and the support structure comprises a plurality of superimposed, contiguous, mutually adhered layers of material.

84. (Previously presented) The semiconductor device assembly of claim 75, wherein the at least one conductive element is located on a surface of each of the first and second semiconductor device components.

85. (Previously presented) The semiconductor device assembly of claim 84, wherein the at least one conductive element extends across a peripheral edge of at least one of the first and second semiconductor device components.

86. (Withdrawn) The semiconductor device assembly of claim 80, further comprising a carrier substrate upon which at least one of the semiconductor dice is disposed.

87. (Withdrawn) The semiconductor device assembly of claim 86, further comprising at least one other conductive element connecting at least one other contact pad of at least one of the semiconductor die to at least one contact pad of the carrier substrate.

88. (Withdrawn) The semiconductor device assembly of claim 87, wherein the at least one other conductive element comprises a plurality of superimposed, contiguous, mutually adhered layers of conductive material.

89. (Withdrawn) The semiconductor device assembly of claim 88, wherein the conductive material comprises a conductive elastomer.

90. (Withdrawn) The semiconductor device assembly of claim 88, wherein the conductive material comprises metal.

91-109. (canceled)

110. (Previously presented) A conductive trace at least partially formed on at least one semiconductor device component, comprising a plurality of superimposed, contiguous, mutually adhered layers, each of the layers comprising the same conductive polymer material, at least a

portion of the conductive trace being configured to extend and conduct electrical signals along a plane which is parallel to a plane in which the at least one semiconductor device component is located.

111. (Previously presented) The conductive trace of claim 110, wherein conductive polymer material comprises a thermoplastic conductive elastomer.

112. (Previously presented) The conductive trace of claim 110, configured to be carried by a single semiconductor device component.

113. (Previously presented) The conductive trace of claim 110, configured to at least partially electrically connect two semiconductor device components.

114. (Previously presented) A semiconductor device comprising:

a semiconductor device component; and

at least one conductive trace carried by the semiconductor device component, the at least one conductive trace including a plurality of superimposed, contiguous, mutually adhered layers, each of the layers comprising the same conductive polymer material, at least a portion of the conductive trace being configured to extend and conduct electrical signals along a plane which is parallel to a plane in which the at least one semiconductor device component is located.

115. (Previously presented) The semiconductor device of claim 114, wherein the at least one conductive trace is substantially entirely carried by the semiconductor device component.

116. (Previously presented) The semiconductor device of claim 115, wherein the semiconductor device component comprises a layer of a carrier substrate.

117. (Previously presented) The semiconductor device of claim 115, wherein the semiconductor device component comprises a dielectric layer disposed on an active surface of a semiconductor die.

118. (Previously presented) The semiconductor device of claim 114, wherein the conductive polymer material comprises a thermoplastic conductive elastomer.

119. (Previously presented) The semiconductor device of claim 114, wherein the at least one conductive trace communicates with a contact of the semiconductor device component.

120. (Previously presented) The semiconductor device of claim 119, wherein the semiconductor device component comprises a carrier substrate.

121. (Previously presented) The semiconductor device of claim 119, wherein the semiconductor device component comprises a semiconductor die.

122. (Previously presented) The semiconductor device of claim 119, wherein the semiconductor device component comprises a packaged semiconductor device.

123. (Previously presented) The semiconductor device of claim 114, wherein the semiconductor device component comprises leads.

124. (Previously presented) The semiconductor device of claim 123, wherein the at least one conductive trace contacts one of the leads.